rewritten into independent form. Claims 3, 4, 6, 8, 9, 12-16 are pending. The discussion below is directed to the rejections made to the remaining claims.

A. CLAIMS 3, 8 AND 12

With respect to the rejection of claims 3, 8 and 12 under 35 U.S.C. § 102(e) over Sakamoto et al., the Examiner alleges that the conductive member 306 shown in Figure 5 is a "conductive *clip holding* said first electrode together with said second electrode ..." as recited in claims 3, 8 and 12. As discussed in Applicants' specification on page 5, line 21, an exemplary "conductive clip" of the present invention has "elasticity for clamping objects." However, Sakamoto et al. is completely silent as to the lead 306 being elastic for clamping purposes (e.g., col. 8, lines 15-18 discloses lead 306 as metal with no further description). Accordingly, it is submitted that Sakamoto et al. does not disclose or suggest a clip that holds objects together as contemplated by the present invention. In order to emphasize this distinction, claims 3, 8 and 12 have been amended to define the "clip" as having "elasticity for clamping".

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Sakamoto et al. does not disclose or suggest, *inter alia*, a "conductive clip having elasticity for clamping objects" as recited in the combination of claims 3, 8 and 12, it is submitted Sakamoto et al. does not anticipate claims 3, 8 and 12.

Based on the foregoing, it is respectfully submitted that claims 3, 8 and 12 are patentable over Sakamoto et al.. Accordingly, it is respectfully requested that the

rejection of claims 3, 8 and 12 under 35 U.S.C. § 102(e) over Sakamoto et al., be withdrawn.

B. CLAIMS 4, 9 AND 13

With respect to the rejection of claims 4, 9 and 13 under 35 U.S.C. § 103 over Sakamoto et al. in view of Whitney, the Examiner admits that Sakamoto et al. does not disclose a "conductive layer" and therefore substitutes the lead 306 with the alleged conductive layer 70/80 of Whitney et al. However, the alleged conductive layer 70/80 does not connect electrodes on opposing sides of a substrate (there is an electrode 60 on only one side of the substrate 90), rendering the alleged conductive layer 70/80 immaterial to the claimed "conductive layer" both structurally and functionally (as well as non-analogous to the lead 306 of Sakamoto et al.). In fact, the alleged motivation at col. 1, lines 26-31 of Whitney relied on by the Examiner (i.e., "increasing reliability ...") is simply a *generalized* statement of purpose of the invention as a whole that is completely independent of the *specific* modification made by the Examiner. That is, the Examiner has not set forth any motivation or rationale from the prior art for making the *specific modification* to Sakamoto et al. of using the alleged "conductive layer" of Whitney (e.g., Whitney does not identify use of the alleged "conductive layer" as a means to "increase reliability ..." etc.).

As is well known in patent law, a *prima facie* showing of obviousness can only be established if the prior art "suggests the desirability" of the proposed combination using ***objective*** evidence. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that Sakamoto et al. can be modified by Whitney (although it appears they are unrelated disclosures), it is submitted that the "mere fact that [Sakamoto et al. and Whitney] can be combined ... does not render the resultant combination obvious" because nowhere does the prior art "suggest the desirability of the combination" as set forth by the Examiner. The examiner has not provided any ***objective*** evidence that the cited prior art suggests the "desirability of the combination" as required for a proper rejection under 35 U.S.C. § 103. Rather, at best, the Examiner attempted to show only that the individual elements of the combination recited in claims 3, 8 and 12 are known in a plurality of different references. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that Sakamoto et al. and Whitney "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no ***objective*** reason on the record to combine the teachings

of the cited prior art. In contrast, Sakamoto et al. and Whitney are completely silent as to providing a rationale or motivation for combining the teachings thereof as set forth by the Examiner. The only motivation set forth by the Examiner to make the proposed combination is an arbitrary statement that the proposed modification is "for the purpose of increasing reliability and operation of the package." However, as noted above, there is no ***objective*** evidence on the record that modifying Sakamoto et al. by using the alleged conductive layer of Whitney would increase reliability. Importantly, the disclosed purpose of Whitney is carried out by constructing the invention therein as a whole, and there is no indication that using the alleged "conductive layer" *by itself* performs the stated purpose.

It is therefore respectfully submitted that the proposed combination is based solely on improper hindsight reasoning, whereby the Examiner selected bits and pieces of the claimed invention and used only Applicants' specification as a guide to reconstruct the claimed invention. Based on the foregoing, it is respectfully submitted that claims 4, 9 and 13 are patentable over Sakamoto et al. in view of Whitney. Accordingly, it is respectfully requested that the rejection of claims 4, 9 and 13 under 35 U.S.C. § 103 over Sakamoto et al. in view of Whitney, be withdrawn.

C. CLAIM 6

With respect to the rejection of claim 6 under 35 U.S.C. § 103 over Sakamoto et al. in view of Gaynes et al., it is respectfully submitted that the Examiner's rejection is based solely on improper hindsight reasoning, where the Examiner picked and chose claimed elements from the various references and used Applicants' specification as a guide to reconstruct the claimed invention (e.g., the arrangement of semiconductors in

Sakamoto et al. does not appear to be amenable to modification by coupling conductive patterns between respective semiconductors, and the motivation for making the combination appears to be contrived by the Examiner). For all the same reasons discussed above in section B with respect to claims 4, 9 and 13, it is submitted that the proposed combination is improper for failing to provide the requisite motivation/rationale from the prior art to make the modifications.

Furthermore, even assuming *arguendo* proper, the proposed combination still does not disclose or suggest each and every limitation of claim 6. Claim 6 recites in pertinent part (through dependency on claim 5) "semiconductor device units [that] are stacked on each other ... ." Accordingly, the stacked relation of claim 5 would be distinguished from the horizontally spaced semiconductors of Sakamoto et al. (i.e., Sakamoto et al. in view of Gaynes et al. does not teach semiconductor device units stacked "on" each other). The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejections fail to "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 6 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Based on the foregoing, it is respectfully submitted that claim 6 is patentable over Sakamoto et al. in view of Gaynes et al.. Accordingly, it is respectfully requested that the

rejection of claim 6 under 35 U.S.C. § 103 over Sakamoto et al. in view of Gaynes et al., be withdrawn.

D. CLAIMS 14-16

1. Akram et al.

With respect to the rejection of claims 14-16 under 35 U.S.C. § 102(b) over Akram et al. (Figures 3 and 4), it appears that the device of Akram et al. does not have electrically connecting electrodes to conductive patterns, whereby the conductive patterns are *electrically connected* to each other as recited in claim 14. In contrast, conductors 26 appear to be *electrically isolated* from each other as shown in Figure 3 of Akram et al..

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Akram et al. does not disclose or suggest, *inter alia*, a "conductive patterns of said spacer members [that] are electrically connected to each other" as recited in 14, it is submitted Akram et al. does not anticipate claim 14, nor any claim dependent thereon.

Based on the foregoing, it is respectfully submitted that claim 14 and its dependent claims 15-16 are patentable over Akram et al.. Accordingly, it is respectfully requested that the rejection of claims 14-16 under 35 U.S.C. § 102(b) over Akram et al., be withdrawn.

Furthermore, with respect to claim 16, it is not clear how the Examiner is interpreting the recited "supporting members". The Examiner merely concludes that Figure 4 illustrates "supporting members" without identifying which element of the device of Sakamoto et al. the Examiner is relying on for making the conclusion.

Moreover, it does not appears that Sakamoto et al. (Figure 4) has any structure that could be construed as the "supporting members" recited in claim 16. Accordingly, it is respectfully submitted that claim 16 is patentable over Akram et al. based on its own merits, in addition to being dependent on novel claim 14.

2. Sugano et al.

With respect to the rejection of claims 14-16 under 35 U.S.C. § 102(b) over Sugano et al. (Figures 46-48), it appears that Sugano et al., similarly to the deficiency of Akram et al. discussed above, does not disclose "conductive patterns [that] are electrically connected to each other" as recited in claim 14. In contrast, conductors 312 are electrically isolated from each other as shown in Figure 48 of Sugano et al..

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Sugano et al. does not disclose or suggest, *inter alia*, a "conductive patterns of said spacer members [that] are electrically connected to each other" as recited in 14, it is submitted Sugano et al. does not anticipate claim 14, nor any claim dependent thereon.

Based on the foregoing, it is respectfully submitted that claim 14 and its dependent claims 15-16 are patentable over Sugano et al.. Accordingly, it is respectfully requested that the rejection of claims 14-16 under 35 U.S.C. § 102(b) over Sugano et al., be withdrawn.

With respect to claim 15, although the alleged "spacer members" 310, 314 arguably define a cavity therebetween, this "cavity" does not accommodate the end portion of the semiconductor chip (*see* Figure 47, where the chip 302 is completely

spaced away from the alleged "spacer members" 310, 314). In order to emphasize this distinction, claim 15 has been amended to set forth that the end portion is located at least partially within the cavity defined by the "spacer members." With respect to claim 16, it is again unclear how the Examiner is relying on Sugano et al. (Figure 46, 47) for disclosing the recited "supporting members", which Sugano et al. does not appear to disclose. Accordingly, it is respectfully submitted that claims 15 and 16 are patentable over Sugano et al. based on their own merits, in addition to being dependent on novel claim 14.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

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APPENDIX

IN THE SPECIFICATION:

Paragraph beginning on page 6, line 26 has been amended as follows:

--In Figs. 4 and 5, reference numeral 8 indicates a conductive material injection-molded over the surfaces of the semiconductor chip 1, 7.--

Paragraph beginning on page 10, line 5 has been amended as follows;

--In Figs. 8 through 10, reference numeral 5 indicates a conductive clip, 5' indicates another conductive clip, 7 indicates one of stacked semiconductor chips, and 7' indicates the other of stacked semiconductor chips. A unit comprising a semiconductor chip 1, 7, surface electrodes 2, 3 or an insulation layer 6, and clip 5 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 11, line 19 has been amended as follows:

--In Figs. 11 through 13, reference numeral 8 indicates a conductive material or conductive layer, and 8' indicates another conductive material or conductive layer. A unit comprising a semiconductor chip 1, 7, surface electrodes 2, 3 or an insulation layer 6, and conductive material 8 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 14, line 8 has been amended as follows:

--Fig. 15 is a sectional view showing a structure of a semiconductor device according to an Eighth Embodiment. A unit comprising a semiconductor chip [1] 7,

surface electrodes 2, insulation layer 6, and clip 5 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 14, line 12 has been amended as follows:

--An element of the semiconductor device of this embodiment is the semiconductor device unit described referring to Fig. 3, in which conductive clips 5 clamping the top-surface electrodes 2 and the insulation layers 6 on the back surface are provided on one end of each of the semiconductor chips [1] 7. Each of the semiconductor chips [1] 7 has a conductive pattern 9 on the top surface, and are placed on a packaging board 10 perpendicularly to the packaging board 10, and the conductive clips 5 are electrically connected and fixed to the conductive patterns 9 on the packaging board 10.--

Paragraph beginning on page 14, line 28 and ending on page 15, line 2 has been amended as follows:

-- Alternatively, in the semiconductor device, the semiconductor chips 7 have top-surface electrodes 2 and insulation layers on the back surfaces which are clamped by conductive clips 5. The [he] conductive clips 5 are extended to at least a side of the chips 1 (i.e., top-back connecting terminal or connecting material) are connected and fixed to the packaging board 10. --

Paragraph beginning on page 15, line 3 has been amended as follows:

--By this, semiconductor chips [1] 7 can be placed at a predetermined angle, such as a right angle, against the packaging board 10, and high-density packaging can be performed.--

Paragraph beginning on page 15, line 8 has been amended as follows:

--Fig. 16 is a sectional view showing a structure of a semiconductor device according to a Ninth Embodiment. A unit comprising a semiconductor chip [1] 7, surface electrodes 2, insulation layer 6 and conductive material 8 is named as a semiconductor device unit in this embodiment.--

Paragraph beginning on page 15, line 29 and ending on page 16, line 4 has been amended as follows:

--Alternatively, in the semiconductor device, the back surface of semiconductor chips [1] 7 is insulation-treated, and top-surface electrodes 2 and insulation layers 6 on the back surfaces are connected by injection-molded conductive materials 8, and the conductive materials 8 formed on at least a side of the chips [1] 7 (i.e., top-back connecting terminal or connecting material) are connected to the packaging board 10.--

Paragraph beginning on page 16, line 23 has been amended as follows:

--In the semiconductor device of this embodiment, a plurality of semiconductor chips [1] 7 having electrodes 2 formed on the major surfaces, and a plurality of insulators (spacers) 12 having conductive patterns 11 on the top surfaces are alternately stacked so

that the electrodes 2 of the semiconductor chips [1] 7 are electrically connected with the conductive patterns 11 of the insulators (spacers) 12, and the conductive patterns 11 of the insulators (spacers) 12 adjacent to each other are placed so as to be electrically connected to each other.--

Paragraph beginning on page 17, line 1 has been amended as follows:

--The insulators (spacers) 12 have cavities for accommodating the end portions of the semiconductor chips [1] 7, and are stacked so that the conductive patterns 11 of the insulators (spacers) 12 adjacent to each other are placed so as to be electrically connected to each other.--

IN THE CLAIMS

Claims 3, 4, 6, 8, 9, 12, 13, and 15 have been amended as follows:

3. (Amended) A semiconductor device [according to claim 1] comprising:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip,

wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer, said conductive clip having elasticity for clamping objects.

4. (Amended) A semiconductor device [according to claim 1] comprising:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip,

wherein each of said conductive [member] members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

6. (Amended) A semiconductor device [according to claim 2] comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked on each other,

wherein a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second electrodes, and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns.

8. (Amended) A semiconductor device [according to claim 5] comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other,

wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer, said conductive clip having elasticity for clamping objects.

9. (Amended) A semiconductor device [according to claim 5] comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other,

wherein each of said conductive [member] members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

12. (Amended) A semiconductor device [according to claim 10] comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

a packaging board for mounting said plurality of semiconductor device units;

wherein said semiconductor device units are placed on said packaging board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board,

wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer, said conductive clip having elasticity for clamping objects.

13. (Amended) A semiconductor device [according to claim 10] comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

a packaging board for mounting said plurality of semiconductor device units;

wherein said semiconductor device units are placed on said packaging board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board,

wherein each of said conductive [member] members is comprised of conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

15. (Amended) The semiconductor device according to claim 14, wherein each of said spacer members has a cavity for accommodating the end portion of said semiconductor chip, said end portion is located at least partially within the cavity.